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Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L1	50	(US-5319395-\$ or US-6233668-\$ or US-6237122-\$ or US-5608892-\$ or US-5875466-\$ or US-5388074-\$ or US-5732278-\$ or US-5818789-\$ or US-5924114-\$ or US-5930518-\$ or US-6181609-\$ or US-4458332-\$ or US-5255383-\$ or US-5886705-\$ or US-5899961-\$ or US-6163832-\$ or US-4953121-\$ or US-5237670-\$ or US-5313594-\$ or US-5448714-\$ or US-5481531-\$ or US-5524234-\$ or US-5524235-\$ or US-5555527-\$ or US-5586282-\$ or US-5684774-\$).did. or (US-5805524-\$ or US-5838604-\$ or US-5860111-\$ or US-5949733-\$ or US-6023440-\$ or US-6055615-\$ or US-4456952-\$ or US-4547849-\$ or US-4845656-\$ or US-4879689-\$ or US-4924426-\$ or US-5206942-\$ or US-5416916-\$ or US-5444858-\$ or US-5537577-\$ or US-5561671-\$ or US-5577229-\$ or US-5579279-\$ or US-5586299-\$ or US-5664149-\$ or US-5698876-\$ or US-5717653-\$ or US-5809273-\$ or US-5831903-\$).did.	USPAT	OR	ON	2006/05/18 18:52
L2	23056335	@ad<"20021004"	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/05/18 18:52
L3	50	L1 and L2	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/05/18 18:52
L4	7	(US-5237670-\$ or US-5313594-\$ or US-5444858-\$ or US-5577229-\$ or US-5586299-\$ or US-5732278-\$ or US-5818789-\$).did.	USPAT	OR	ON	2006/05/18 18:52
L5	4	(US-5818789-\$ or US-5732278-\$ or US-5313594-\$ or US-5237670-\$).did.	USPAT	OR	ON	2006/05/18 18:52
L6	4	(US-5818789-\$ or US-5732278-\$ or US-5313594-\$ or US-5237670-\$).did.	USPAT	OR	ON	2006/05/18 18:52
L7	23056335	@ad<"20021004"	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/05/18 18:52
L8	31449	address adj line	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/05/18 18:52
L9	639	(transmit or transmits or transmitted or transmitting) with data with L8	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/05/18 18:52

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L10	29321	memory adj module	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/05/18 18:52
L11	21	L9 same L10	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/05/18 18:52
L12	8	L7 and L11	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/05/18 18:52
L13	19	(transmit or transmits or transmitted or transmitting) with write adj data with L8	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/05/18 18:52
L14	13	L7 and L13	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/05/18 18:52
L15	1	(US-6438634-\$.did.	USPAT	OR	ON	2006/05/18 18:52
L16	29321	memory adj module or memory adj modules	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/05/18 18:52
L17	21	L9 same L16	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/05/18 18:52
L18	21	L8 same L17	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/05/18 18:52
L19	0	L6 and L9	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/05/18 18:52
L20	5632	711/118,169,5,149,154.ccls.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/05/18 19:00

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L21	17	L9 and L20	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/05/18 18:52
L22	17	L7 and L21	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/05/18 18:52
L23	3	(US-6748505-\$ or US-5091845-\$ or US-4851991-\$).did.	USPAT	OR	ON	2006/05/18 18:52
L24	10317	365/189.01,189.05,230.03,230.08.ccls.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/05/18 18:52
L25	21	L7 and L24 and L9	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/05/18 18:52
L26	0	L16 and L25	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/05/18 18:52
L27	21	memory and L25	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/05/18 18:52
L28	2983	((address adj line or address adj lines or address adj bus or address adj buss or address adj busses) near5 (write or writes)) same (memory))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/05/18 18:58
L29	4	13 and 28	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/05/18 18:58
L30	2	2 and 29	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/05/18 18:59
L31	1858	711/118.ccls.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/05/18 19:00

## EAST Search History

L32	0	29 and 31	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/05/18 19:00
L33	488	711/118.ccls.	US-PGPUB	OR	ON	2006/05/18 19:00
L34	202	2 and 33	US-PGPUB	OR	ON	2006/05/18 19:01
L35	0	28 and 34	US-PGPUB	OR	ON	2006/05/18 19:01

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IEEE STD IEEE Standard

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- ☐ 1. **Adaptive approaches for fault detection and diagnosis of interconnects of random access memories**  
Zhao, J.; Meyer, F.J.; Lombardi, E.;  
[Memory Technology, Design and Testing, 1998. Proceedings. International Workshop on](#)  
24-25 Aug. 1998 Page(s):110 - 116  
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- ☐ 2. **Maximal diagnosis of interconnects of random access memories**  
Jun Zhao; Meyer, F.J.; Lombardi, F.; Park, N.;  
[Reliability, IEEE Transactions on](#)  
Volume 52, Issue 4, Dec. 2003 Page(s):423 - 434  
Digital Object Identifier 10.1109/TR.2003.821928  
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- ☐ 3. **Maximal diagnosis of interconnects of random access memories**  
Jun Zhao; Meyer, F.J.; Lombardi, F.;  
[VLSI Test Symposium, 1999. Proceedings. 17th IEEE](#)  
25-29 April 1999 Page(s):378 - 383  
Digital Object Identifier 10.1109/VTEST.1999.766692  
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- ☐ 4. **IEEE standard for information technology -Test methods for measuring conformance to POSIX - part 2: shell and utilities**  
[IEEE Std 2003.2-1996](#)  
1997 Page(s):0\_1 - 1396  
[AbstractPlus](#) | Full Text: [PDF](#)(5120 KB) IEEE STD
- ☐ 5. **IEEE standard for a versatile backplane bus: VMEbus**  
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- ☐ 6. **IEEE standard for an 8-bit microcomputer bus system: STD bus**  
[IEEE Std 961-1987](#)  
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- ☐ 7. **Fault diagnosis of RAMs from random testing experiments**  
David, R.; Fuentes, A.;  
[Computers, IEEE Transactions on](#)  
Volume 39, Issue 2, Feb. 1990 Page(s):220 - 229  
Digital Object Identifier 10.1109/12.45207  
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- ☐ 8. **IEEE Standard Microcomputer System Bus**  
[ANSI/IEEE Std 796-1983](#)  
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- ☐ 9. **The Sun Fireplane System Interconnect**  
Charlesworth, A.;  
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- ☐ 10. **An American National Standard IEEE Standard For Mechanical Core Specifications for Microcomputers**  
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- ☐ 11. **Testing Interconnections to static RAMs**  
Bhavsar, D.K.;  
[Design & Test of Computers, IEEE](#)  
Volume 8, Issue 2, June 1991 Page(s):63 - 71  
Digital Object Identifier 10.1109/54.82039  
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- ☐ 12. **Designing the PowerPC 60X bus.**  
Allen, M.S.; Alexander, M.; Wright, C.; Chang, J.;  
[Micro, IEEE](#)  
Volume 14, Issue 5, Oct. 1994 Page(s):42  
Digital Object Identifier 10.1109/MM.1994.363068  
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- ☐ 13. **Standard for Information technology - portable operating system interface (POSIX). Shell and utilities**  
[IEEE Std 1003.1, 2004 Edition. The Open Group Technical Standard. Base Specifications, Issue 6. Includes IEEE Std 1003.1-2001, IEEE Std 1003.1-2001/Cor 1-2002 and IEEE Std 1003.1-2001/Cor 2-2004. Shell and Utilities 2004](#)  
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- ☐ 14. **Standard for Information Technology - Portable Operating System Interface (POSIX) Shell and Utilities, Issue 6**  
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- ☐ 15. **Concurrency, latency, or system overhead: Which has the largest impact on uniprocessor DRAM-system performance?**  
Cuppu, V.; Jacob, B.;  
[Computer Architecture, 2001. Proceedings. 28th Annual International Symposium on](#)  
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-  **16. IEEE standard for multiplexed high-performance bus structure: VSB**  
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-  **18. IEEE Standard 696 Interface Devices**  
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-  **19. AC-and DC-powered subnanosecond 1-kbit Josephson cache memory design**  
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[Solid-State Circuits, IEEE Journal of](#)  
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-  **20. Power estimation for architectural exploration of HW/SW communication on system-level buses**  
Fornaciari, W.; Sciuto, D.; Silvano, C.;  
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-  **21. A high-speed 64K/spl times/4 CMOS DRAM using on-chip self-timing techniques**  
Kobayashi, T.; Arimoto, K.; Ikeda, Y.; Hatanaka, M.; Mashiko, K.; Yamada, M.; Nakano, T.;  
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Volume 21, Issue 5, Oct 1986 Page(s):655 - 661  
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-  **22. An experimental 220-MHz 1-Gb DRAM with a distributed-column-control architecture**  
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Volume 30, Issue 11, Nov. 1995 Page(s):1165 - 1173  
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-  **23. Concurrent fault simulation on message passing multicomputers**  
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-  **24. A case for studying DRAM issues at the system level**  
Jacob, B.;  
[Micro, IEEE](#)

Volume 23, Issue 4, July-Aug. 2003 Page(s):44 - 56

Digital Object Identifier 10.1109/MM.2003.1225969

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**25. Automated bus generation for multiprocessor SoC design**

Kyeong Keol Ryu; Mooney, V.J., III;

[Computer-Aided Design of Integrated Circuits and Systems, IEEE Transactions on](#)

Volume 23, Issue 11, Nov. 2004 Page(s):1531 - 1549

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### 1. On the value locality of store instructions

Lepak, K.M.; Lipasti, M.H.;  
[Computer Architecture, 2000. Proceedings of the 27th International Symposium on](#)  
2000 Page(s):182 - 191

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### 2. Silent stores and store value locality

Lepak, K.M.; Bell, G.B.; Lipasti, M.H.;  
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Volume 50, Issue 11, Nov. 2001 Page(s):1174 - 1190  
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### 3. An algorithm to test reconfigured RAMs

Franklin, M.; Saluja, K.K.;  
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Digital Object Identifier 10.1109/ICVD.1994.282719

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### 4. Defect analysis and realistic fault model extensions for static random access memories

Zarrineh, K.; Deo, A.P.; Adams, R.D.;  
[Memory Technology, Design and Testing, 2000. Records of the 2000 IEEE International Workshop on](#)  
7-8 Aug. 2000 Page(s):119 - 124  
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### 5. A 500 ps 32 × 8 register file implemented in GaAs/AlGaAs HBTs [F-RISC/G processor]

Nah, K.; Philhower, R.; Greub, H.; McDonald, J.F.;  
[Gallium Arsenide Integrated Circuit \(GaAs IC\) Symposium, 1993. Technical Digest 1993., 15th Annual](#)  
10-13 Oct. 1993 Page(s):71 - 74  
Digital Object Identifier 10.1109/GAAS.1993.394497

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### 6. A novel slotted-ring architecture for parallel processing: an application

Yaremchuk, G.; Pon, C.R.; Kwasniewski, T.; Goubran, R.;

Electrical and Computer Engineering, 1994. Conference Proceedings. 1994 Canadian Conference on  
25-28 Sept. 1994 Page(s):486 - 489 vol.2

Digital Object Identifier 10.1109/CCECE.1994.405794

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 Jun Zhao; Meyer, F.J.; Lombardi, F.; Park, N.;  
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[Computers, IEEE Transactions on](#)  
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 Digital Object Identifier 10.1109/12.966493  
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- 4. Testing reconfigured RAM's and scrambled address RAM's for pattern sensitive faults**  
 Franklin, M.; Saluja, K.K.;  
[Computer-Aided Design of Integrated Circuits and Systems, IEEE Transactions on](#)  
 Volume 15, Issue 9, Sept. 1996 Page(s):1081 - 1087  
 Digital Object Identifier 10.1109/43.536714  
[AbstractPlus](#) | [References](#) | Full Text: [PDF](#)(708 KB) IEEE JNL  
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- 5. Maximal diagnosis of interconnects of random access memories**  
 Jun Zhao; Meyer, F.J.; Lombardi, F.;  
[VLSI Test Symposium, 1999. Proceedings. 17th IEEE](#)  
 25-29 April 1999 Page(s):378 - 383  
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- 6. A 500 ps 32 × 8 register file implemented in GaAs/AlGaAs HBTs [F-RISC/G processor]**

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Gallium Arsenide Integrated Circuit (GaAs IC) Symposium, 1993. Technical Digest 1993., 15th Annual  
10-13 Oct. 1993 Page(s):71 - 74  
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Digital Object Identifier 10.1109/ICVD.1994.282719  
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**8. A novel slotted-ring architecture for parallel processing: an application**

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